FORM PTO-1390
REV. 5-93

US DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEYS DOCKET NUMBER
P00,0578

U.S.APPLICATION NO. (if known, see 37 CFR 1.5)
09/530553

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE98/03197	**November 2, 1998**	**November 3, 1997**

TITLE OF INVENTION **HIGH VOLTAGE RESISTANT EDGE STRUCTURE FOR SEMICONDUCTOR COMPONENTS**

APPLICANT(S) FOR DO/EO/US **GERALD DEBOY, JENOE TIHANYI, HELMUT STRACK, HELMUT GASSEL, JENS-PEER STENGL and HANS WEBER**

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay.
4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of International Application (35 U.S.C. 371(c)(2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2).

7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. §371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)) **(attached at back of English translation of application).**

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98; **(PTO 1449, Prior Art, Search Report)**.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.
    (SEE ATTACHED ENVELOPE)

13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

be
. ☐ A substitute specification.

S
15. ☐ A change of power of attorney and/or address letter.

16. ☒ Other items or information:
    a. ☒ Submission of Drawings
    b. ☒ Request for Approval of Drawing Changes
    c. ☒ EXPRESS MAIL #EL482397091US

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IN THE UNITED STATES DESIGNATED/ELECTED OFFICE

OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER THE PATENT COOPERATION TREATY-CHAPTER II

AMENDMENT "A" PRIOR TO ACTION

APPLICANT(S):	Gerald Deboy et al.
ATTORNEY DOCKET NO.:	P00,0578
INTERNATIONAL APPLICATION NO.:	PCT/DE98/03197
INTERNATIONAL FILING DATE:	02 November 1998
INVENTION:	"HIGH VOLTAGE RESISTANT EDGE STRUCTURE FOR SEMICONDUCTOR COMPONENTS"

Assistant Commissioner for Patents

Washington, D.C. 20231

Sir:

Applicants herewith amend the above-referenced PCT application, and request entry of the Amendment prior to examination in the United States National Examination Phase.

IN THE SPECIFICATION:

On page 1, cancel the title above line 3, and insert the following above line 3:

--TITLE

HIGH VOLTAGE RESISTANT EDGE STRUCTURE FOR SEMICONDUCTOR COMPONENTS

BACKGROUND OF THE INVENTION--;

in line 3, after "The" insert --present--;

in line 4, cancel "according to the preamble of Patent Claim 1";

in line 8, cancel "the" substitute --a-- therefor;

in line 10, preceding "second" cancel "the" substitute --a-- therefor;

in line 20, cancel "patent" substitute --Patent No.-- therefor;

in line 25, cancel "US" substitute --United States Patent No.-- therefor.

On page 2, in line 4, cancel "US" substitute --United States Patent No.-- therefor;

in line 6, cancel "plurality" substitute --number-- therefor;

in line 9, insert a centered heading:

--**<u>SUMMARY OF THE INVENTION</u>**--;

cancel lines 15-16, substitute the following at line 15:

-- This object is inventively achieved in accordance with the present invention in a high voltage resistant edge structure in an edge region of a semiconductor component, said edge structure comprising:

a semiconductor body having at least one inner zone of a first conductivity type adjacent to a first surface of said semiconductor body;

at least one floating guard ring of a second conductivity type arranged in said inner zone; and

inter-ring zones of said first conductivity type respectively arranged in said inner zone, said inter-ring zones being allocated in pairs to each of said floating guard rings, said inter-ring zones being arranged laterally such that they separate two respective consecutive floating guard rings from one another,

wherein at least one of said floating guard rings and said inter-ring zones have at least one of conductivities and geometries set such that their free charge carriers are totally depleted when a blocking voltage is applied.--.

On page 3, in line 10, cancel "Beyond this" substitute --In an embodiment-- therefor;

in line 11, cancel "particular" substitute --an embodiment-- therefor;

in line 21, cancel "The" substitute --In an embodiment-- therefor;

in line 23, cancel ", respectively,";

in line 26, cancel "What" substitute --In an embodiment, what-- therefor;

in line 29, cancel ", or respectively," substitute --or-- therefor.

On page 4, in line 2, cancel "As" substitute --In an embodiment, as-- therefor;

in line 4, cancel "Depending" substitute --In an embodiment, depending-- therefor, and cancel "it would also be imaginable";

in line 5, cancel "to realize", and after "stopper" insert --is realized--;

in line 7, cancel ", respectively";

in line 9, cancel "The" substitute --In an embodiment, the-- therefor;

in line 11, cancel "It" substitute --In an embodiment, is-- therefor.

On page 5, cancel lines 5-25, substitute the following at line 5:

-- In an embodiment, at least an outermost of the magnetoresistors is nearly completely enclosed by a cathode metallization in a direction of the first surface of the semiconductor component.

In an embodiment, the cathode metallization is a metallization of a source electrode of the semiconductor component.

In an embodiment, the inter-ring zones in the edge region have a cross-section tapered to the first surface.

In an embodiment, the semiconductor component is one of a vertical power transistor or an IGBT.

These and other features of the invention(s) will become clearer with reference to the following detailed description of the presently preferred embodiments and accompanied drawings.

DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-section of a high voltage resistant semiconductor component, which is constructed as a D-MOSFET (or IGBT) here and which comprises an edge structure constructed in accordance with the present invention.

Figure 2 is a cross-section of a further embodiment of an inventive edge structure constructed in accordance with the present invention.

Figure 3 shows several cross-sections representing various trench types.

Figure 4 shows several exemplifying embodiments representing the creation of a homogeneous doping distribution in the edge region of a semiconductor component, which can be purposefully adjusted.

Figure 5 shows several cross-sections representing various edge variations for adjusting a purposeful, "softly" leaking doping concentration in the edge region of a semiconductor component.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS--.

On page 6, in line 1, cancel "subsection" substitute --cross-section-- therefor;

in line 4, cancel "consisting of a plurality" substitute --having a number-- therefor.

On page 7, in line 1, cancel "plurality" substitute --number-- therefor;

in line 15, after "IGBT" cancel ", respectively", and after "zones 8" cancel ", respectively,";

in line 17, cancel ", respectively";

in line 19, cancel ", respectively";

in line 22, after "10' " insert --(not labelled)--.

On page 8, in line 1, cancel ", respectively".

On page 9, in line 24, cancel "subsection" substitute --cross-section-- therefor;

in line 28, cancel "121" substitute --11-- therefor.

On page 10, in line 2, cancel ", or respectively," substitute --or-- therefor;

in line 6, cancel ", or respectively," substitute --or-- therefor;

in line 20, cancel "btwen [sic]" substitute --between-- therefor.

On page 11, in line 1, cancel "trechn [sic]" substitute --trench-- therefor, and cancel "subsection" substitute --cross-section-- therefor;
in line 3, cancel "trechn [sic]" substitute --trench-- therefor;
in line 5, cancel "The" substitute --In the-- therefor;
in line 13, cancel "subsection" substitute --cross-section-- therefor.

On page 12, in line 9, cancel "development" substitute --embodiment-- therefor.

On page 13, in line 6, cancel ", or respectively," substitute --or-- therefor;
in line 9, cancel ", or respectively," substitute --or-- therefor;
in line 19, cancel "It would also be imaginable" substitute --In an embodiment, it is possible-- therefor;
in line 22, cancel "use" substitute --be used-- therefor;
in line 23, cancel "[sic]";
in line 27, after "grid" cancel the comma;
in line 28, cancel "respectively,".

On page 14, in line 12, cancel ", or respectively," substitute --or-- therefor;
below line 13, insert the following paragraph:

-- Although modifications and changes may be suggested by those of ordinary skill in the art, it is the intention of the inventors to embody within the patent warranted hereon all changes and modifications as reasonably and properly come within the scope of their contribution to the art.--.

Cancel page 15.

IN THE CLAIMS:

On page 16, in line 1, cancel "Patent Claims" substitute --**WE CLAIM AS OUR INVENTION:**-- therefor.

Please cancel claims 1-15.

Please add the following new claims 16-30:

16. A high voltage resistant edge structure in an edge region of a semiconductor component, said edge structure comprising:

a semiconductor body having at least one inner zone of a first conductivity type adjacent to a first surface of said semiconductor body;

at least one floating guard ring of a second conductivity type arranged in said inner zone; and

inter-ring zones of said first conductivity type respectively arranged in said inner zone, said inter-ring zones being allocated in pairs to each of said floating guard rings, said inter-ring zones being arranged laterally such that they separate two respective consecutive floating guard rings from one another,

wherein at least one of said floating guard rings and said inter-ring zones have at least one of conductivities and geometries set such that their free charge carriers are totally depleted when a blocking voltage is applied.

17. The high voltage resistant edge structure as claimed in claim 16, wherein at least one of a width of said inter-ring zones increases in a direction of said semiconductor component and a width of said floating guard rings decreases in a direction of an edge of said semiconductor component.

18. The high voltage resistant edge structure as claimed in claim 16, wherein at least one of said floating guard rings and said inter-ring zones respectively comprise a same width.

19. The high voltage resistant edge structure as claimed in claim 16, wherein a depth of said floating guard rings deceases in a direction of an edge of said semiconductor component.

20. The high voltage resistant edge structure as claimed in claim 16, wherein said floating guard rings have one of a U-shaped or V-shaped cross-section.

21. The high voltage resistant edge structure as claimed in claim 16, further comprising:

at least one space charge zone stopper located at an outermost edge of said edge region of said semiconductor component.

22. The high voltage resistant edge structure as claimed in claim 21, wherein said space charge zone stopper comprises a heavily doped region of said first conductivity type, said heavily doped region being arranged in said inner zone.

23. The high voltage resistant edge structure as claimed in claim 21, wherein said space charge zone stopper comprises a damage implanted region being arranged in said inner zone.

24. The high voltage resistant edge structure edge as claimed in claim 21, wherein said space charge zone stopper comprises an electrode connected to said inner zone, said electrode being one of metallic or containing polysilicon.

25. The high voltage resistant edge structure as claimed in claim 16, further comprising:

at least one magnetoresistor located at an inner edge of said edge region of said semiconductor component.

26. The high voltage resistant edge structure as claimed in claim 25, wherein at least one of said magnetoresistors is simultaneously a gate electrode of said semiconductor component.

27. The high voltage resistant edge structure as claimed in claim 25, wherein at least an outermost of said magnetoresistors is nearly completely enclosed by a cathode metallization in a direction of said first surface of said semiconductor component.

28. The high voltage resistant edge structure as claimed in claim 27, wherein said cathode metallization is a metallization of a source electrode of said semiconductor component.

29. The high voltage resistant edge structure as claimed in claim 16, wherein said inter-ring zones in said edge region have a cross-section tapered to said first surface.

30. The high voltage resistant edge structure as claimed in claim 16, wherein said semiconductor component is one of a vertical power transistor or an IGBT.

IN THE ABSTRACT:

On page 19, cancel lines 1-3, insert the following centered heading at line 1:

--**ABSTRACT OF THE DISCLOSURE**--;

in line 5, cancel "The invention relates to a" substitute --A-- therefor;

in line 6, cancel "the" substitute --a-- therefor;

in line 7, after "of" cancel "the" substitute --a-- therefor;

cancel line

REMARKS:

The present Amendment revises the specification, drawings and claims to conform to United States patent practice, before examination of the present PCT application in the United States National Examination Phase. All of the changes are editorial and no new matter is added thereby. Claims 1-15 have been canceled. New claims 16-30 are patentably distinguishable from the known prior art.

Early examination on the merits is respectfully requested.

Respectfully submitted,

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IN THE UNITED STATES DESIGNATED/ELECTED OFFICE

OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER THE PATENT COOPERATION TREATY-CHAPTER II

REQUEST FOR APPROVAL OF DRAWING CHANGES

APPLICANT(S):	Gerald Deboy et al.
ATTORNEY DOCKET NO.:	P00,0578
INTERNATIONAL APPLICATION NO.:	PCT/DE98/03197
INTERNATIONAL FILING DATE:	02 November 1998
INVENTION:	"HIGH VOLTAGE RESISTANT EDGE STRUCTURE FOR SEMICONDUCTOR COMPONENTS"

Assistant Commissioner for Patents

Washington, D.C. 20231

S I R:

Applicant herewith requests approval of the drawing changes in FIGs. 4A, 4B, 4C and 4D as shown on the drawing copies marked in red attached hereto.

Submitted by,

(Reg. 31,870)

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FIG 4A

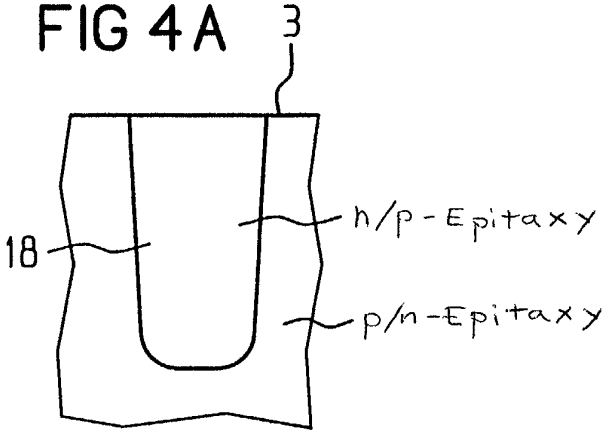


FIG 4B

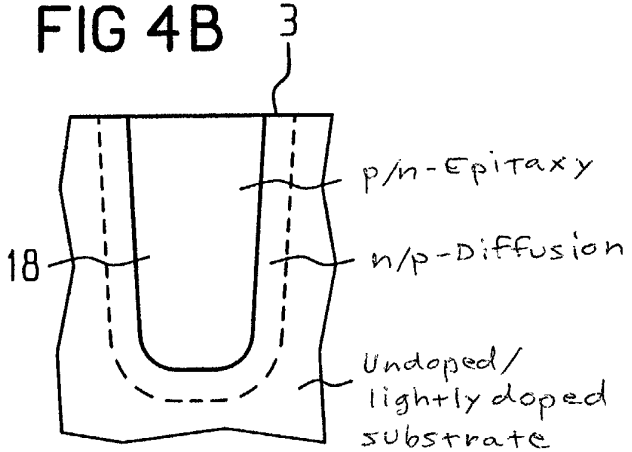


FIG 4C

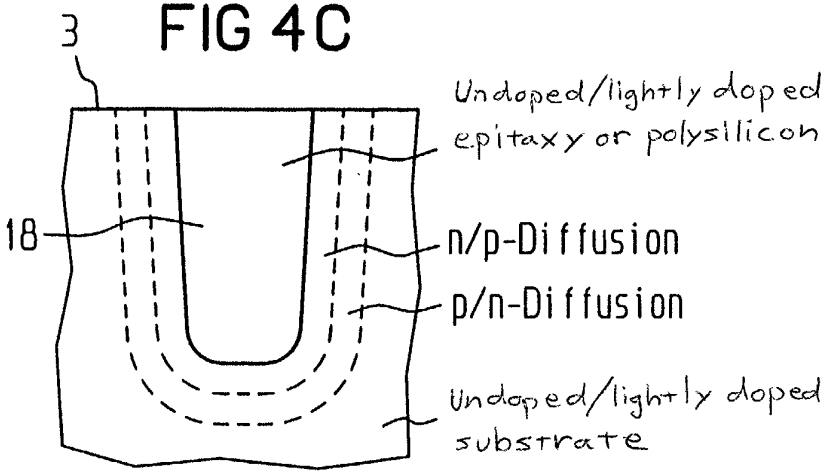
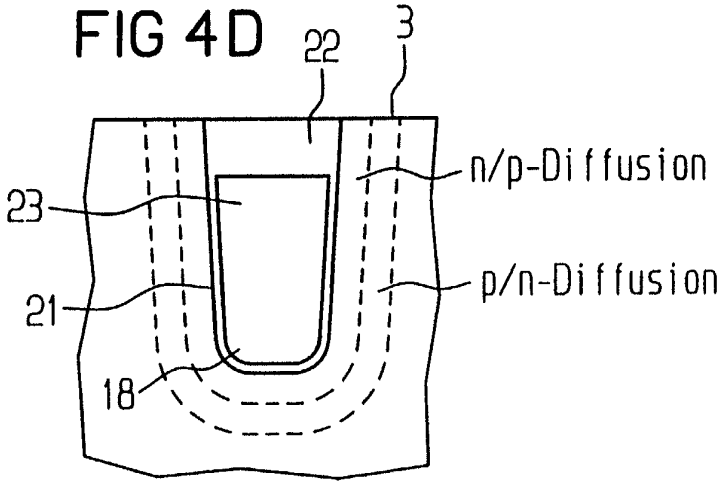


FIG 4D



High Voltage Resistant Edge Structure for Semiconductor Components

The invention relates to a high voltage resistant edge structure in the edge region of a semiconductor component according to the preamble of Patent Claim 1.

Accordingly, a high voltage resistant edge structure in the edge region of a semiconductor component is provided, which has a semiconductor body, at whose first surface at least one inner zone of the first conductivity type is adjacent, at least one floating guard ring arranged in the inner zone, and at least one inter-ring zone of the second conductivity type arranged between the floating guard rings.

In semiconductor elements, particularly in high voltage resistant power semiconductor components, voltage breakthroughs preferably arise in their edge region outside the doping zones, since the electrical field intensity is especially great there due to the curvature of the doping zones which is conditioned by the edge. To avoid such voltage breakthroughs, doping zones are arranged in rings about the semiconductor components. These annular doping zones reduce local field intensity peaks in the edge region of the semiconductor component.

Such protective rings are described in the Canadian patent 667,423, for example. But since the field intensity must be reduced to almost zero in each of the guard rings, the floating guard rings described there must be dimensioned very wide toward the edge. This edge structure consumes a great deal of space, accordingly.

Furthermore, US 3,405,329 teaches edge structures of semiconductor components with what are known as magnetoresistive rings. These magnetoresistive rings are constructed so as to achieve a largely uniform voltage distribution along the surface of the semiconductor body of a semiconductor component. In this way, field intensity peaks which favor the occurrence of a breakthrough are avoided. The realization of

these magnetoresistive rings in the edge region of the semiconductor component is likewise very costly in terms of space.

US 4,468,686 teaches a high voltage resistant edge structure with magnetoresistive rings and annular doping zones arranged under the magnetoresistive rings. These annular doping zones essentially consist of a plurality of cascaded MOS transistors. The design of this edge structure likewise takes up a large amount of space in the edge region of the semiconductor component.

Proceeding on the basis of this prior art, it is the object of the present invention to set forth a simple and space-efficient embodiment of a high voltage resistant edge structure for semiconductor components, which further ensures a breakthrough voltage at a reproducible level.

This object is inventively achieved by an edge structure of the species which has the features of the Patent Claim 1.

Accordingly, a species-related edge structure is provided, in which the conductivities and/or geometries of the floating guard rings and/or the inter-ring zones are set such that their charge carriers are totally depleted when blocking voltage is applied.

The inventive edge structure achieves a modulation of the electrical field both at the surface and in the volume of the semiconductor. With appropriate dimensioning of the inventive edge structure, the field strength maximum can be easily shifted into the depth of the semiconductor body; that is, into the region of the vertical p-n junction. Thus, there can always be a suitable design for an edge structure over a wide range of concentrations of p and n doping, which design allows a "soft" leakage of the electrical field in the volume.

In a particularly advantageous embodiment of the present invention, the floating guard rings have the same width, whereby the width of the inter-ring zones arranged between the individual floating guard rings increases in the direction of the edge of the semiconductor component.

In a further advantageous embodiment, the width of the floating guard rings decreases in the direction of the edge of the semiconductor component, and the inter-ring zones between the individual floating guard rings have the same width, respectively.

Beyond this, the depth of the floating guard rings can be varied in the direction of the edge of the semiconductor component. In particular, it is advantageous when the depth of the floating guard rings decreases in the direction of the edge of the semiconductor component.

Accordingly, the remaining design parameters for the inventive edge structure include the widths, spacings, and depths of the floating guard rings, which can be defined using lithographic masks. An optimal edge structure can thus be designed for any semiconductor component, and particularly for an arbitrary range of blocking voltages of semiconductor components, using realistically simple means.

The subsection of the floating guard rings advantageously has a trench-shaped cross-section in the shape of a V or U. The V-shaped or U-shaped form of the cross-section, can be produced easily by an isotropic or anisotropic etching process, respectively, and a subsequent deposition process.

What is known as a space charge region stopper is also located in the edge region of the semiconductor component. Space charge region stopper refers to an electrode or a heavily doped diffusion zone in the outermost edge region, which defines the lateral extent of the space charge zone beyond the floating guard rings, or respectively,

defines the electrical field. The space charge region stopper usually provides at least a multiple of the breakthrough charge as breakthrough voltage. As space charge region stopper, a heavily doped zone of the same conductivity type as the epitaxial layer can be provided. Depending on the respective requirements, it would also be imaginable to realize the space charge region stopper as what is known as a "damage-implanted" region (implantation zone) or as a metal electrode that is shorted to the substrate material of the semiconductor body, respectively.

The inventive edge structure is expediently provided with at least one magnetoresistor in the direction of the edge, which guarantees the component a good electrostatic protection against mobile parasitic charges in its housing. It has also proven expedient to lead the cathode electrode (in MOSFETs their source electrode), which is situated adjacent the edge structure, up vertically in the direction of the edge region – that is, out of the semiconductor body – in order to allow the electrical field to escape from the semiconductor body.

For the overall edge structure, the corresponding design parameters derive from the maximum permissible electrical field and relate essentially to a boundary surface charge that falls safely below the maximum in the region of the vertically extending p-n junctions. In silicon, this maximum boundary surface charge is approx. 1.5×10^{12} cm^{-2}. Thus, a given doping profile of the semiconductor body in the edge region results in a layout that is rather simple to manage. The shift of the field strength maximum into the region of the transitions between the individual floating guard rings and inter-ring zones arranged between them is achieved by a net excess of acceptor atoms over the entire surface. This means that, over the whole surface, the sum of the implanted dopants in the floating guard rings must exceed the sum of the doping in the intervening inter-ring zones.

Compared to a conventional edge structure, the inventive edge structure can be dimensioned up to 33% smaller in its lateral extent in the direction of the edge of the semiconductor body.

Further advantageous developments of the invention derive from the respective subclaims.

The invention is detailed below with the aid of the exemplifying embodiments indicated in the Figures. Shown are:

Figure 1 a subsection of a high voltage resistant semiconductor component, which is constructed as a D-MOSFET (or respectively, IGBT) here and which comprises an inventive edge structure;

Figure 2 a subsection of a further inventive edge structure;

Figure 3 several subsections representing various trench types;

Figure 4 several exemplifying embodiments representing the creation of a homogenous doping distribution in the edge region of a semiconductor component, which can be purposefully adjusted;

Figure 5 several subsections representing various edge variations for adjusting a purposeful, "softly" leaking doping concentration in the edge region of a semiconductor component.

To the extent that they are not referenced otherwise, elements that are the same or that have the same function are provided with the same reference characters in all Figures of the drawing.

Figure 1 shows a subsection of a high voltage resistant (power) semiconductor component comprising an inventive edge structure.

The semiconductor component comprises a cell field ZF consisting of a plurality of individual components, which are connected in parallel and are arranged in individual cells Z1...Z3, of which the outermost three cells Z1...Z3 are represented as cutouts only. The cell field ZF is terminated by an edge structure that is provided in the edge region RB of the semiconductor component. The edge region RB refers to the region of the semiconductor component located outside its active cells Z1...Z3 of the cell field ZF.

In Figure 1, the semiconductor body of the semiconductor component is referenced 1. The semiconductor body 1, which consists of silicon substrate, for example, comprises an n-doped inner zone 2 in this embodiment, which is situated adjacent the first surface 3 of the semiconductor body 1 at the source side. The inner zone 2 is typically deposited onto the semiconductor body 1 by an epitaxy process. Particularly in high voltage resistant power semiconductor components having a very high blocking voltage, this epitaxy layer is created with the aid of several consecutive epitaxy steps, wherein a respective epitaxial sublayer is deposited on top of the layer below it. This technique is known as the build-up technique.

At the drain side, a drain zone 4 is adjacent the inner zone 2. If the semiconductor component is constructed as a MOSFET, then the drain zone 4 is typically heavily n-doped. But if the semiconductor component is an IGBT, then the drain zone 4 is also designated as an anode zone and is typically heavily p-doped (represented by brackets in Figure 1). In this case, the boundary surface 5 characterizes the p-n junction between the drain zone 4 and the inner zone 2. Beyond this, the drain zone 4 is adjacent the second surface 6 of the semiconductor body 1 and is connected here surface-wide to the drain electrode 7 and thus to the drain terminal D.

At the source-side surface 3, a plurality of base zones 8 are embedded in the inner zone 2. The base zones 8 comprise the opposite conductivity type to the inner zone 2; that is, they are p-doped in the present case. In the present exemplifying embodiment, at least one heavily n-doped source zone 9 is embedded in each of the base zones 8, respectively. In the present exemplifying embodiment, the base zones 8 and the source zones 9 embedded in them have a trough shape and can be created by ion implantation and/or by diffusion, for example.

The base zones 8 and/or the source zones 9 typically, though not necessarily, have the same cell design as the corresponding cells Z1...Z3 in which they are embedded. Such a cell design can consist of cells in the shape of strips, hexagons, triangles, quadrilaterals, circles, ovals, or some such.

The semiconductor component in Figure 1 is constructed as a vertical D MOSFET (or IGBT, respectively). Of course, the source zones 9 or the base zones 8, respectively, can also be arranged in what is known as a trench. The corresponding semiconductor component would then be a trench MOSFET or a trench IGBT, respectively. It would also be imaginable to give the source zones 9 or the base zones 8 a V-shaped or trapezoidal cross-section, respectively.

In Figure 1, the source zones 9 and the base zones 8 are connected in known fashion to the source electrode 10, and thus to the source terminal S, via contact holes 10'. This shunting of the base zone 8 and the source zone 9 makes it possible to keep a parasitic bipolar transistor from being turned on there.

Beyond this, a gate electrode 11 that is insulated from the semiconductor body 1 via a thin gate oxide 12 is provided at the first surface 3. The gate electrode 11 is connected to the gate terminal G and can consist of heavily doped polysilicon or

metal, respectively. A field oxide 13 is further provided, which insulates the source electrode 10 from the gate electrode 11 and from the semiconductor body 1.

Finally, the semiconductor component according to Figure 1 has a space charge zone stopper 14. This space charge zone stopper 14 is arranged at the outermost edge region RB of the semiconductor component; that is, directly before its arris. In the present exemplifying embodiment, the space charge zone stopper 14 is constructed in known fashion as a single-stage metal electrode 14' that rises in the direction of the cell field ZF, which is contacted to a heavily n-doped diffusion zone 14". The metal electrode 14' can also be constructed as a polysilicon electrode, or can be omitted, depending on the application.

Typically, stepped magnetoresistive rings 17 are provided in the edge region Rb of a power semiconductor. Such magnetoresistors 17 are typically single-step or multi-step, these magnetoresistors 17 leading away from the first surface 3 in the direction of the edge. In the exemplifying embodiment according to Figure 1, only one single-step magnetoresistor 17 is shown.

For reasons of optimizing surface area, it has proven advantageous that the gate electrodes 11 of the respectively outermost cells Z1 of the active cell field ZF simultaneously take over the function of the magnetoresistor 17. It has also proven advantageous that the source electrode 10 adjacent the edge structure is likewise led up vertically in the direction of the edge; that is, is led up from the first surface 3 of the semiconductor body 1. This allows the electrical field to escape from the semiconductor body 1.

Guard rings 15 are inventively provided in the edge region RB; that is, outside the active cell field ZF. These guard rings 15, which are lightly p-doped in this exemplifying embodiment, are "floating"; that is, they have an undefined potential. In

the subsection in Figure 1, these floating guard rings 15 are columnar and extend from the first surface 3 of the semiconductor body 1 to deep in the inner zone 2. In the exemplifying embodiment according to Figure 1, four of these floating guard rings 15 are provided.

The floating guard rings 15 are spaced apart from one another, and the region between the floating guard rings 15 defines an inter-ring zone 16. This inter-ring zone 16 typically, though not necessarily, has the same dopant concentration as the sub-base doping; that is, as the inner zone 2. The lateral and horizontal dimensions and geometries of the floating guard rings 15 and inter-ring zones 16 and their dopant concentration are not discussed further here. These points are described later with the aid of Figures 3 to 5.

The inter-ring zones 16 are typically produced by what is known as the trench technique. In the present exemplifying embodiment, the trenches of the inter-ring zones 16 extend from the first surface 3 of the semiconductor body 1 deep into the inner zone 2. Of course, it would also be possible for these trenches 16 to extend through the entire inner zone 2 and to connect to the drain zone 4. In principle, it is also conceivable for the trenches 16 to penetrate from the first surface 3 to the second surface 6 at the back of the wafer of the semiconductor body. This situation is described later with the aid of Figure 5.

Figure 2 illustrates another exemplifying embodiment of an inventive edge structure with reference to a subsection.

In Figure 2, the inter-ring zones 16 are additionally tapered in the direction of the first surface 3 of the semiconductor body. Furthermore, it is particularly advantageous when the source electrode 10 encompasses the corresponding gate electrode 121 in the direction of the edge region RB. That is, the source electrode 10 projects in the

direction of the edge region RB beyond the corresponding outermost gate electrode 11, or respectively, the magnetoresistor 17, and is then taken down again in the direction of the first surface 3 of the semiconductor body 1.

The result of this is a structure in the edge structure RB wherein the outermost gate electrode 11, or respectively, magnetoresistor 17, is approximately located in a Faraday cage and thus in a nearly field-free space. Compared to the conventional edge structure that is described in Figure 1, wherein the source electrode 10 is merely drawn up to ever thicker oxide layers of the field oxide 13 in the direction of the edge, the source electrode 10 that encompasses the gate electrode 11 achieves a significant reduction of the electrical field that is directed to the corresponding gate electrode 11.

By virtue of the above described tapering of the annular inter-ring zones 16 to the first surface 3, the electrical field intensity at the end of the metallization of the source electrode 10 can be reduced to below the respective field intensity of the volume. In a complete reversal of the previous design, the metal electrode 14' of the space charge zone stopper 14 in the outermost region of the edge structure can thus be additionally drawn up onto at least one second oxide step of the field oxide 13. In this way, the electrical field distribution in the open area OB of the edge structure – that is, in the region btwen **[sic]** the space charge zone stopper 14 and the magnetoresistor 17 – is so modified that the field lines of the electrical field can emerge from the semiconductor body 1 at the first surface 3 via the entire open area OB nearly unchanged by the respective electrodes 14', 17. In this way, the diffusion zone 14″ under the metal electrode 14' an be significantly reduced in the direction of the gate electrode 11 and of cell field ZF. The width of the above cited open area OB between the space charge zone stopper 14 and the outermost cell Z1 of the cell field ZF can thus be significantly reduced, which leads to a considerable reduction of the surface-area of the inventive edge structure and thus of the corresponding semiconductor component.

In Figure 3, several trechn **[sic]** types are shown in subsection.

To create the inter-ring zones 16 with the aid of the trechn **[sic]** technique, trenches 18 are etched into the inner zone 2 of the semiconductor body 1. In Figure 1 and Figure 3(a), these trenches 18 are constructed in an ideally columnar fashion. The present exemplifying embodiment, the trenches 18 have a bottom 19 that runs approximately parallel to the first surface 3, and walls 20 that are ideally arranged at a right angle to the first surface 3. Typically, however, these walls 20 are angled at a flank angle α relative to the horizontal, forming a trench 18 with an approximately trapezoidal cross-section which tapers into the depth of the semiconductor body 1 (Figure 3(b)). But this is not absolutely necessary. It would also be conceivable for the trenches 18 to have a cross-section in the form of trenches that are shaped like a V (Figure 3(c)) or a U (Figure 3(d)) in subsection.

A few preferred methods for producing a homogenous doping distribution that can be purposefully adjusted in the edge region of a semiconductor component, and thus for producing an inventive edge structure, are described below with the aid of Figure 4. In all subfigures 4(a)-(d) only one individual trench 18 is represented, for the sake of providing a better overview.

Trenches 18 in the form of points, strips, or grids are etched into a relatively heavily doped base material of a first conductivity type, for instance into the inner zone 2 (Figure 4(a)). The trenches 18 are epitaxially filled with material of the second conductivity type. Here, the overall charge is set such that a net doping over the whole surface area is approximately zero, and the surface charge does not exceed the breakthrough charge in any spatial direction. A net doping of close to zero means that the number of acceptors (holes) and the number of donators (electrons) in the lateral projection are approximately in balance.

In another embodiment of the present invention, trenches 18 in the form of strips, points, or grids are etched into a lightly doped or undoped base material (Figure 4(b)). Next, the trenches 18 are covered with epitaxially deposited silicon, polycrystalline silicon or boric phosphorous silicate glass with a doping of the first conductivity type. The doping is driven into the surrounding base material; for instance, by a thermal process. The coating is subsequently etched away again. Next, the trenches 18 are filled again with an epitaxially deposited silicon of the second conductivity type.

In an advantageous development, it is also possible to drive the doping of the second conductivity type into the surrounding base material via a coating and a subsequent thermal step (Figure 4(c)). In this case, to achieve a definite separation of the two conductivity zones, dopants with sharply differing diffusion coefficients should be used. The advantage of this procedure is that, given the failure of a trench 18, for instance, due to a particle during the lithography process, the semiconductor component remains fully functional. In the first method cited, on the other hand, this can give rise to a breakdown of the blocking voltage in this region, and thus to the failure of the whole semiconductor component.

Instead of filling the trenches 18 with epitaxially deposited silicon, a hollow space 23 can remain in the trenches, as long as the walls 20 are covered by a passivation layer 21 and the hollow space 2, 3 is occluded on top by a lid 22, for instance consisting of boric phosphorous silicate glass (BPSG) (Figure 4(d)).

Figure 5 shows several subsections, with the aid of which different variants of the edge for setting a purposeful, "softly" leaking doping concentration in the edge region of a semiconductor component are represented. In Figure 5, for the sake of a better overview, the structures corresponding to the Figures 1 and 2 were represented only schematically, since what is essential here is the geometry, the dimensions and the

spacings of the trenches 18, particularly in the edge region RB of the semiconductor component.

The trenches 18 can be etched proceeding from the first surface 3, ideally in a self-aligning manner with respect to the actual component processing (for instance, aligned to the polysilicon edge), or proceeding from the back, or respectively, the second surface 6, after the semiconductor body 1 has been ground thin. Anisotropic etching or isotropic etching can be used. In principle, the trenches 18 may also penetrate from the first surface 3 to the back, or respectively, the second surface 6 (Figure 5(a)). If these trenches 18 are doped sufficiently heavily, the relatively expensive epitaxy wafers can be forgone.

By varying the depth of the trenches 18 in the direction of the edge (Figure 5(a) and (c)), it is possible to favorably influence the field intensity distribution in the edge region RB . In Figure 5(c), the depth t1>t2>t3 of the trenches 18 diminishes continuously in the direction of the edge. In the cell field ZF of the component, the location of the voltage breakthrough can thus be specified.

It would also be imaginable to vary the dopant coating of the trenches in the radial or vertical direction (Figure 5(b)). For example, if trenches 18 with a V-shaped cross-section and an epitaxial filling of these trenches 18 are used, then the shape of the trenches 18 can intentionally use for vertical variation of the implanted charge proportion **[sic].** In particular, the flank angle α of the trench walls can also increase in the direction of the edge.

To achieve an optimally gradual transition of the doping from nearly fully compensated to significantly n or p doped, it is possible either to enlarge the grid, or respectively, the spacings (d1>d2>d3>d4) of two neighboring trenches 18, in the

direction of the edge in a gradual manner (Figure 5(d)), or to reduce the diameter (r1>r2>r3>r4>R5) of the trenches 18 in the direction of the edge (Figure 5(e)).

Compared to the initially cited build-up technique, the trench technique, as it is referred to, using etched tenches 18 has the advantage that smaller cell grids can be provided. These smaller cell grids can then comprise a heavier doping, thereby reducing the surface make resistance $R_{DS,ON}$ significantly.

By way of conclusion, it should be expressly stated that it is of course possible to apply any of the structures described in the Figures 3 to 5 alone or, rather advantageously, in combination with one another, in order to achieve the desired doping profile, or respectively, the desired surfacewide doping distribution, in the edge region RB.

Reference Characters

1	semiconductor body
2	inner zone
3	first surface
4	drain zone
5	boundary surface, p-n junction
6	second surface
7	drain electrode
8	base zone
9	source zone
10	source electrode
10'	contact hole for the source electrode
11	gate electrode
12	gate oxide
13	field oxide
14	space charge zone stopper
14'	metal electrode of the space charge zone stopper
14″	diffusion region of the space charge zone stopper
15	(floating) guard rings
16	inter-ring zones
17	magnetoresistor
18	trenches
19	bottom of trenches
20	wall of trench
21	passivation layer in the trench
22	trench lid
23	hollow space
α	flank angle of the trench wall
d1...d4	spacing between two adjacent trenches, trench grid
r1...r5	trench diameter
t1...t3	trench depth
OB	open area in the edge region
RB	edge region
Z1...Z3	cells
ZF	cell field
D	drain terminal
G	gate terminal
S	source terminal

Patent Claims

1. High voltage resistant edge structure in the edge region (RB) of a semiconductor component

- having a semiconductor body (1), at whose first surface (3) at least one inner zone (2) of the first conductivity type is adjacent,
- having at least one floating guard ring (15) of the second conductivity type arranged in the inner zone (2), and
- having inter-ring zones (16) of the first conductivity type respectively arranged in the inner zone (2), which are allocated in pairs to each floating guard ring (15), these inter-ring zones being arranged laterally such the **[sic]** they separate two respective consecutive floating guard rings (15) from one another,

characterized in that

the conductivities and/or the geometries of the floating guard rings (15) and/or of the inter-ring zones (16) are set such that their free charge carriers are totally depleted when blocking voltage is applied.

2. High voltage resistant edge structure as claimed in claim 1,

characterized in that

the width (r1...r5) of the inter-ring zones (16) increases in the direction of the semiconductor component and/or the width (d1...d4) of the floating guard rings (15) decreases in the direction of the edge of the semiconductor component.

3. High voltage resistant edge structure as claimed in one of the preceding claims,

characterized in that

the floating guard rings (15) or the inter-ring zones (16) respectively comprise the same width.

4. High voltage resistant edge structure as claimed in one of the preceding claims,

characterized in that

the depth (t1...t3) of the floating guard rings (15) deceases in the direction of the edge of the semiconductor component.

5. High voltage resistant edge structure as claimed in one of the preceding claims, characterized in that

the floating guard rings (15) have a U-shaped or V-shaped cross-section.

6. High voltage resistant edge structure as claimed in one of the preceding claims, characterized in that

at the outermost edge of the edge region (RB) of the semiconductor component, at least one space charge zone stopper (14,14',14″) is provided.

7. High voltage resistant edge structure as claimed in claim 6, characterized in that

the space charge zone stopper (14,14',14″) has a heavily doped region (14″) of the first conductivity type that is arranged in the inner zone (2).

8. High voltage resistant edge structure as claimed in one of the claims 6 or 7, characterized in that

the space charge zone stopper (14,14',14″) has a damage implanted region (14″) that is arranged in the inner zone (2).

9. High voltage resistant edge structure edge structure **[sic]** as claimed in one of the claims 6 to 8, characterized in that

the space charge zone stopper (14,14',14″) has an electrode (14') that is metallic or that contains polysilicon, which is connected to the inner zone (2).

10. High voltage resistant edge structure as claimed in one of the preceding claims, characterized in that
at least one magnetoresistor (17) is provided at the inner edge of the edge region (RB) of the semiconductor component.

11. High voltage resistant edge structure as claimed in claim 10,
characterized in that
at least one of the magnetoresistors (17) is simultaneously a gate electrode (11) of the semiconductor component.

12. High voltage resistant edge structure as claimed in one of the claims 10 to 12,
characterized in that
at least the outermost magnetoresistor (17) is nearly completely enclosed by a cathode metallization (10) in the direction of the first surface (3) of the semiconductor component.

13. High voltage resistant edge structure as claimed in claim 12,
characterized in that
the cathode metallization (10) is the metallization of the source electrode (10) of the semiconductor component.

14. High voltage resistant edge structure as claimed in one of the preceding claims,
characterized in that
the cross-section of the inter-ring zones (16) in the edge region (RB) is constructed so as to be tapered to the first surface (3).

15. High voltage resistant edge structure as claimed in one of the preceding claims,
characterized in that
the semiconductor component is a vertical power transistor or an IGBT.

Abstract

High Voltage Resistant Edge Structure for Semiconductor Components

The invention relates to a high voltage resistant edge structure in the edge region of a semiconductor component which has floating guard rings of the first conductivity type and inter-ring zones of the second conductivity type which are arranged between the floating guard rings, wherein the conductivities and/or the inter-ring zones are set such that their charge carriers are totally depleted when blocking voltage is applied. The inventive edge structure achieves a modulation of the electrical field both at the surface and in the volume of the semiconductor body. If the inventive edge structure is suitably dimensioned, the field intensity maximum can easily be situated in the depth; that is, in the region of the vertical p-n junction. Thus, a suitable edge construction which permits a "soft" leakage of the electrical field in the volume can always be provided over a wide range of concentrations of p and n doping.

Figure 2

FIG 1

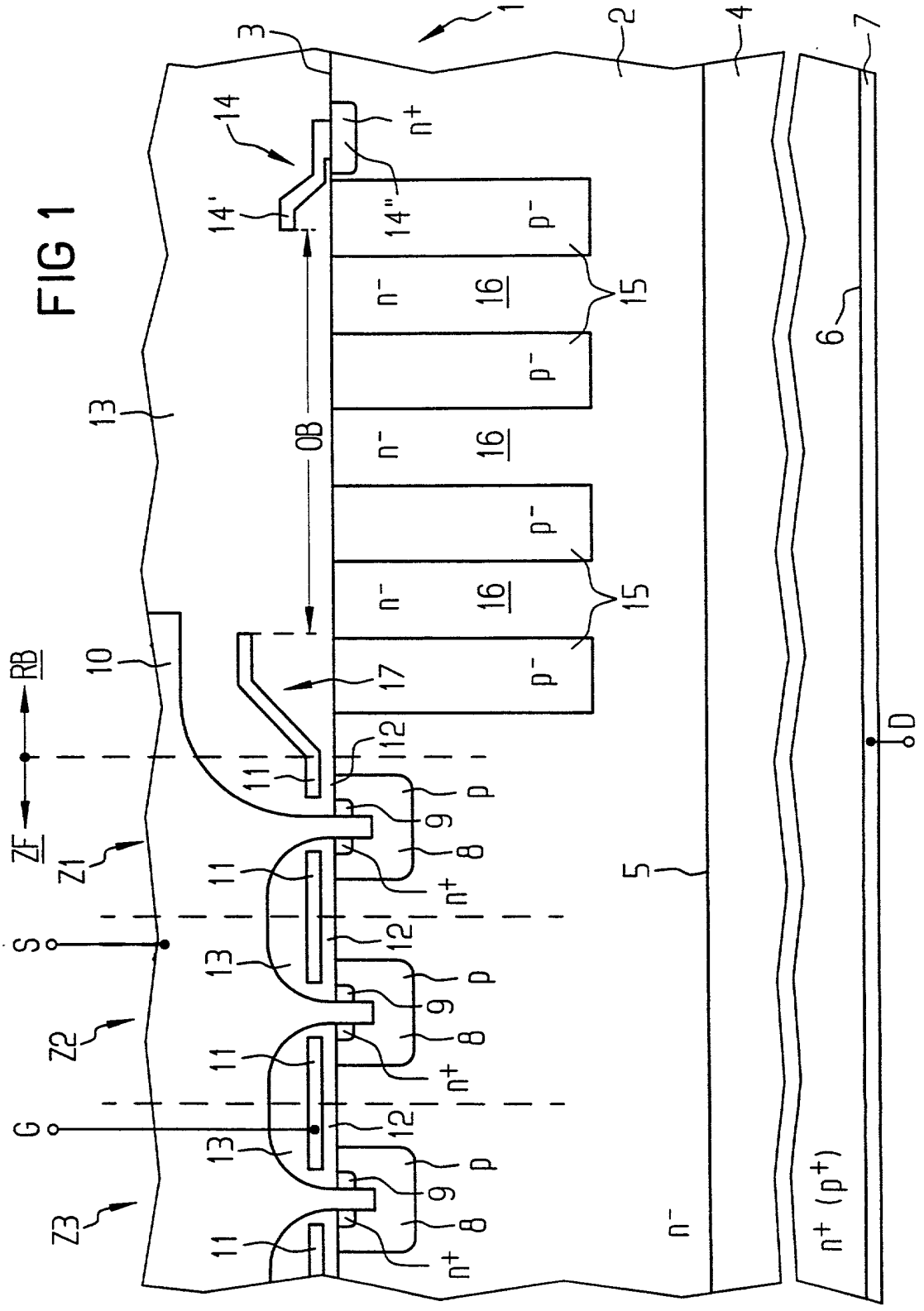
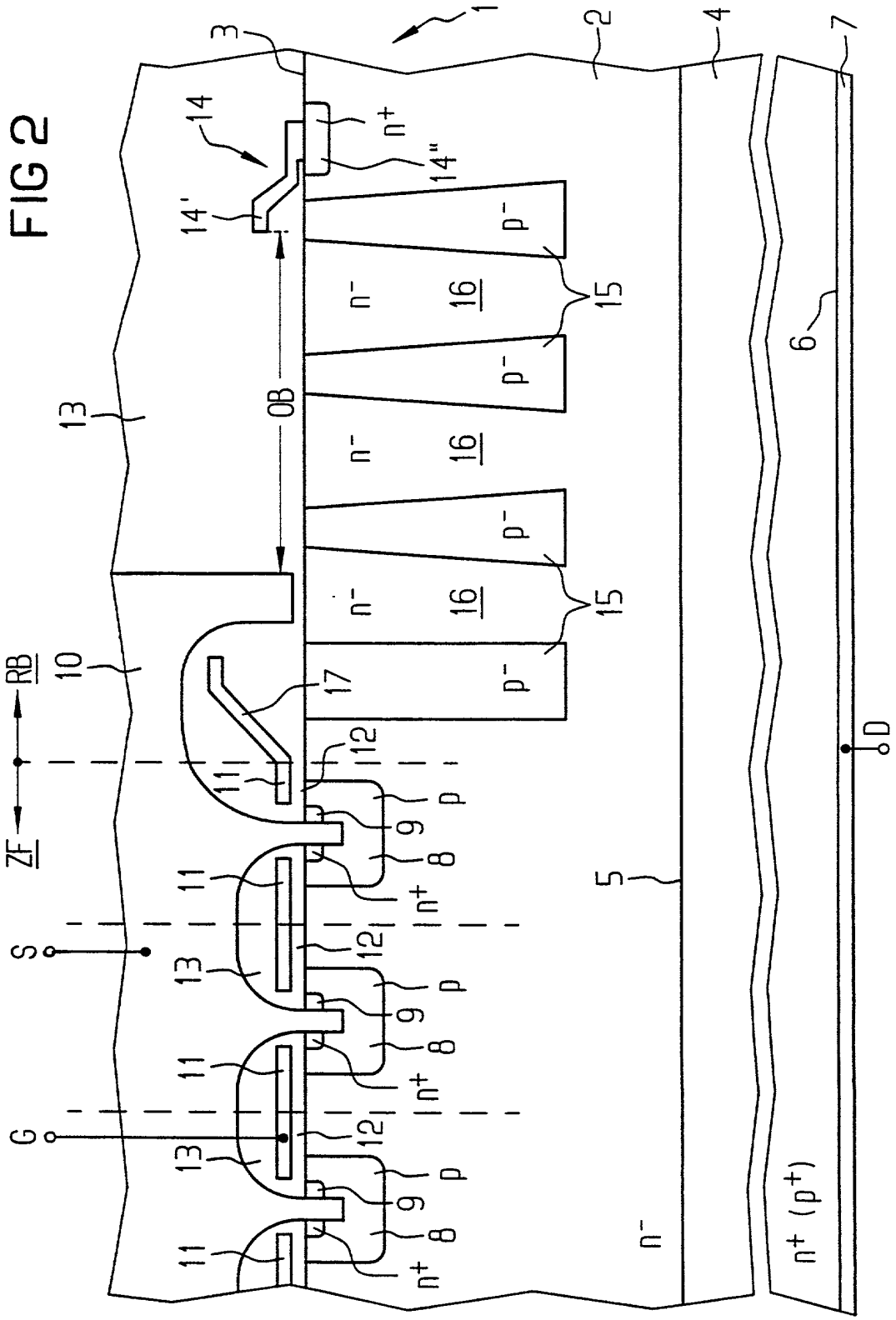


FIG 2



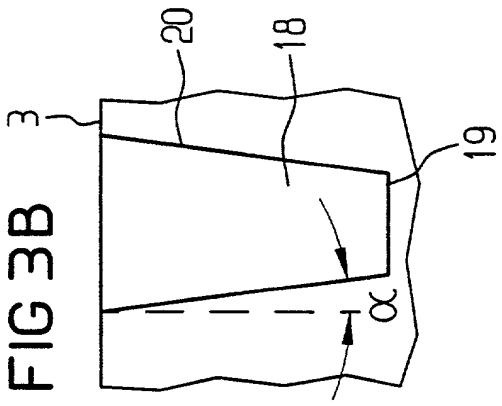


FIG 3B

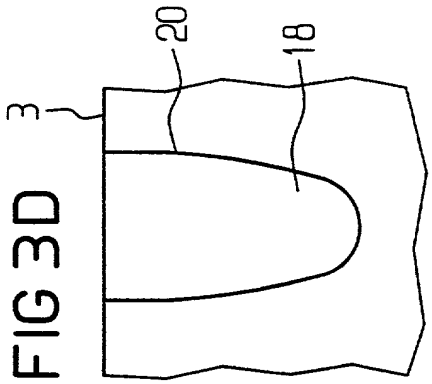


FIG 3D

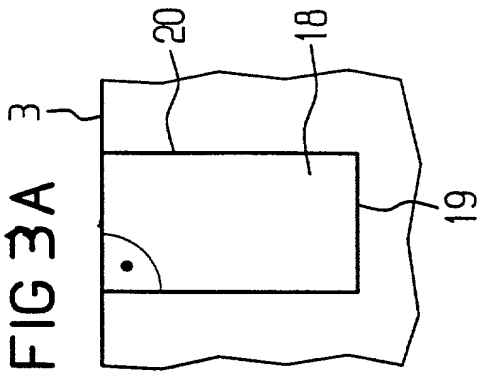


FIG 3A

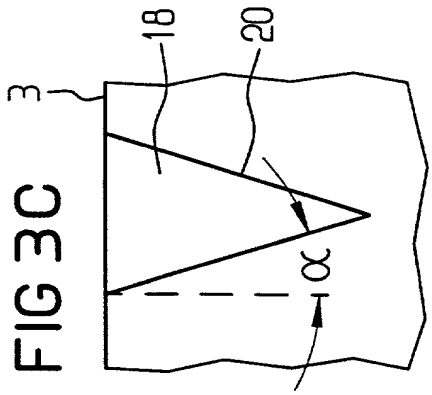


FIG 3C

FIG 4A

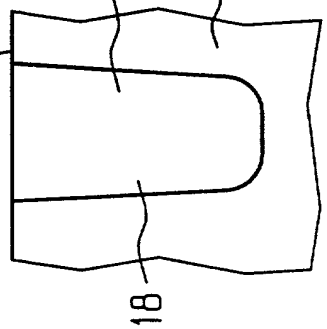


FIG 4B

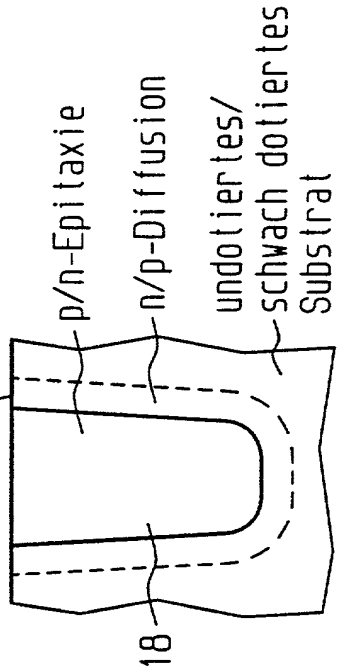


FIG 4C

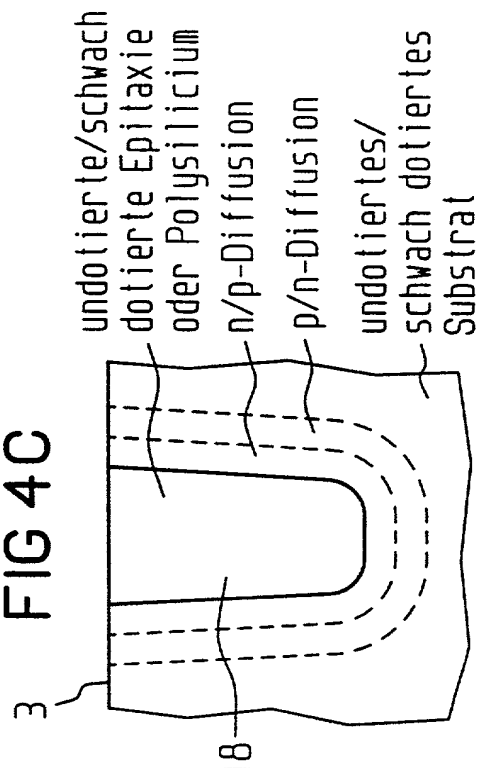


FIG 4D

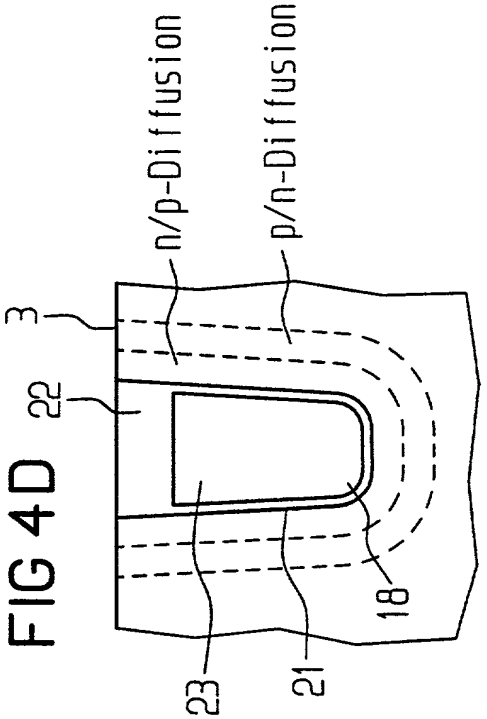


FIG 5A

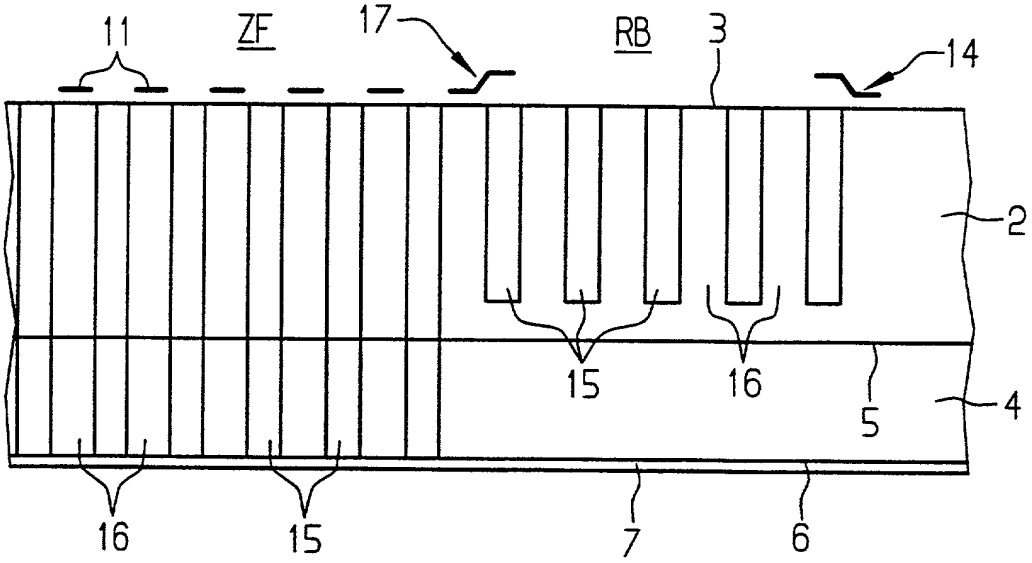


FIG 5B

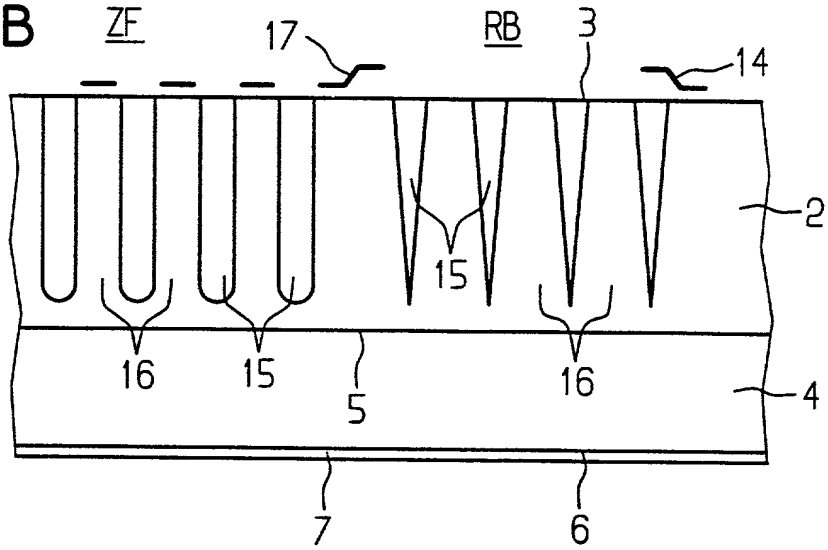


FIG 5C

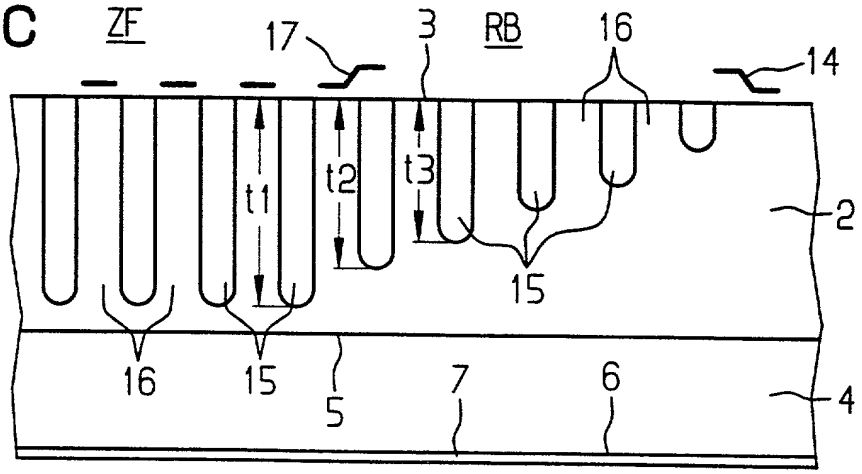


FIG 5D

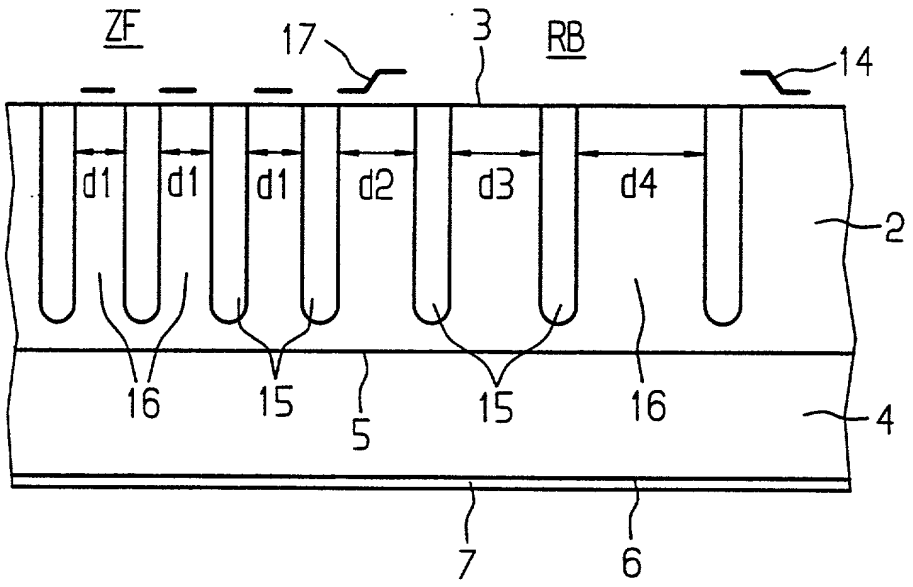
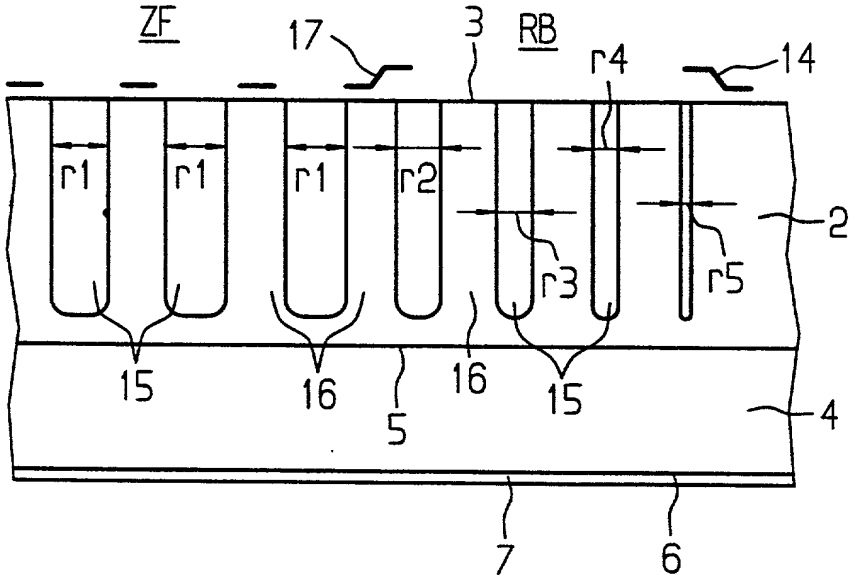

ZF
17
3
RB
14
d1
d1
d1
d2
d3
d4
2
16
15
5
15
16
4
7
6

FIG 5E


ZF
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RB
r4
14
r1
r1
r1
r2
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r3
r5
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German Language Declaration

Prior foreign applications Priorität beansprucht			Priority Claimed	
197 48 524.3	Germany	3.11.1997	☒	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein
_____	_____	_____	☐	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein
_____	_____	_____	☐	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein

Ich beanspruche hiermit germäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

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(Application Serial No.) (Anmeldeseriennummer)	(Filing Date) (Anmeldedatum)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
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(zutreffendes ankreuzen)

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☒am 9.4.1998 als
PCT internationale Anmeldung
PCT Anmeldungsnummer PCT/DE98/01038
eingereicht wurde und am _____
abgeändert wurde (falls tatsächlich abgeändert).

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I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

HIGH VOLTAGE RESISTANT EDGE STRUCTURE FOR SEMICONDUCTOR COMPONENTS

the specification of which

(check one)

☐ is attached hereto

☒ was filed on November 2, 1998, ✓ as
PCT international application
PCT Application No. PCT/DE98/03197✓
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

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And I hereby appoint Messrs. John D. Simpson (Registration No. 19,842), Dennis A. Gross (24,410), Robert M. Barrett, (30,142), Steven H. Noll (28,982), Kevin W. Guynn (29,927), Robert M. Ward (26,517), Brett A. Valiquet (27,841), Edward A. Lehman (22,312), David R. Metzger (32,919), James D. Hobart (24,149), Melvin A. Robinson (31,870), Joseph P. Reagen (35,332), Michael R. Hull (35,902), Michael S. Leonard (37,557), William E. Vaughan (39,056) and Lewis T. Steadman (17,074), all members of the firm of Hill & Simpson, A Professional Corporation

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A Professional Corporation
85th Floor Sears Tower, Chicago, Illinois 60606

Voller Name des einzigen oder ursprünglichen Erfinders: Gerald Deboy	Full name of sole or first inventor:
Unterschrift des Erfinders: Gerald D. Datum: 31.5.00	Inventor's signature Date
Wohnsitz: ~~Unterhaching, Germany~~ Munich, Germany DEX	Residence
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(Bitte entsprechende Informationen und Unterschriften im Falle von weiteren Miterfindern angeben).

(Supply similar information and signature for subsequent joint inventors).

Voller Name des zweiten Miterfinders (falls zuttreffend): 2-00 Jenoe Tihanyi	Full name of second joint inventor, if any:
Unterschrift des Erfinders Jenoe Tihanyi Datum 2x6.00	Inventor's signature Date
Wohnsitz Kirchheim, Germany DEX	Residence
Staatsangehörigkeit German	Citizenship
Postanschrift Isarweg 13	Post Office Addre
D-85551 Kirchheim Bundesrepublik Deutschland	
Voller Name des dritten Miterfinders (falls zuttreffend): 3-00 Helmut Strack	Full name of third joint inventor, if any:
Unterschrift des Erfinders Helmut Strack Datum 8.6.00	Inventor's signature Date
Wohnsitz Muenchen, Germany DEX	Residence
Staatsangehorigkeit ~~German~~ Austrian	Citizenship
Postanschrift Speyerer Strasse 6	Post Office Address
D-80804 Muenchen Bundesrepublik Deutschland	
Voller Name des vierten Miterfinders (falls zuttreffend): 4-00 Helmut Gassel	Full name of fourth joint inventor, if any:
Unterschrift des Erfinders H Gassel Datum 27.6.2000	Inventor's signature Date
Wohnsitz ~~Muenchen, Germany~~	Residence FARMINGTON HILLS, MI, USA MI
Staatsangehorigkeit German	Citizenship GERMAN
Postanschrift ~~Sperberstrasse 20~~	Post Office Address 37007 ASHOVER CT.
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(Bitte entsprechende Informationen und Unterschriften im Falle von zweiten und weiteren Miterfindern angeben).

(Supply similar information and signature for second and subsequent joint inventors).

Voller Name des zweiten Miterfinders (falls zuttreffend): 5-02 Jens-Peer Stengl	Full name of fifth joint inventor, if any:
Unterschrift des Erfinders ~~des Erfinders~~ Datum Jens-Peer Stengl 26.06.2000	Inventor's signature Date
Wohnsitz Grafrath, Germany ~~DEX~~	Residence
Staatsangehörigkeit ~~German~~ Österreichisch	Citizenship
Postanschrift Kirchfeldstrasse 6	Post Office Address
D-82284 Grafrath Bundesrepublik Deutschland	
Voller Name des dritten Miterfinders (falls zuttreffend): 6-02 Hans Weber	Full name of sixth joint inventor, if any:
Unterschrift des Erfinders Datum Hans Weber 13.06.2000	Inventor's signature Date
Wohnsitz Ainring, ~~Switzerland~~ Germany ~~DEX~~	Residence
Staatsangehörigkeit German	Citizenship
Postanschrift Saalachau 112	Post Office Address
D-83404 Ainring ~~Switzerland~~ Germany	
Voller Name des vierten Miterfinders (falls zuttreffend):	Full name of seventh joint inventor, if any:
Unterschrift des Erfinders Datum	Inventor's signature Date
Wohnsitz	Residence
Staatsangehörigkeit Bundesrepublik Deutschland	Citizenship
Postanschrift	Post Office Address
Bundesrepublik Deutschland	

(Bitte entsprechende Informationen und Unterschriften im Falle von zweiten und weiteren Miterfindern angeben).

(Supply similar information and signature for second and subsequent joint inventors).